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(54) SOLID-STATE IMAGE PICK-UP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solid-state image pick-up device, which solves the problem of rise in the reverse bias voltage to discharge the electric charge stored in the photoelectric converter and which controls blooming between the adjacent photoelectric converters.

SOLUTION: This solid-state image pick-up device is provided an n-type semiconductor substrate 24, a p-type well 27 placed in the middle part of the depth from the surface of 24, photodiodes which are arranged in the form of a matrix on the upper part of the n-type semiconductor substrate 24 and which generates stored charge corresponded to the incident light, and an element isolation region 23 formed between photodiodes 22. In the element isolation region 23, the first p-type element isolation impurity diffusion layer 30 is mounted, and the second p-type element isolation impurity diffusion layer 31 is mounted immediately below it with a clearance.

CLAIMS

[Claim(s)]

[Claim 1]A semiconductor substrate.

A photoelectric conversion part which is provided so that it may become

predetermined arrangement in the upper part of said semiconductor substrate,

and generates stored charge according to incident light.

An isolation region which separates this photoelectric conversion part.

The 1st impurity diffused layer that discharges excess charges by which it was generated in said photoelectric conversion part to the exterior.

It is the solid state image pickup device provided with the above, and said isolation region is provided with the 3rd impurity diffused layer under the 2nd impurity diffused layer and said 2nd impurity diffused layer.

[Claim 2]The solid state image pickup device according to claim 1, wherein a photoelectric conversion part is arranged in the shape of two dimensions, and the 3rd impurity diffused layer is provided so that a directly under field of said photoelectric conversion part may be surrounded.

[Claim 3]The solid state image pickup device according to claim 2, wherein the 3rd impurity diffused layer is formed in a prescribed depth part from the surface in a semiconductor substrate in the shape of an approximately lattice.

[Claim 4]The solid state image pickup device according to claim 1, wherein a position which shows maximum peak concentration in an impurity profile of the 2nd impurity diffused layer is a position and an approximately same depth position which show the maximum potential of a photoelectric conversion part.

[Claim 5]The solid state image pickup device according to claim 1, wherein the 3rd impurity diffused layer is provided in a position of depth direction distance of

approximately middle of the 2nd impurity diffused layer and the 1st impurity diffused layer.

[Claim 6]The solid state image pickup device according to claim 1, wherein the 3rd impurity diffused layer serves as the same pattern as the 2nd impurity diffused layer.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the solid state image pickup device which has vertical mold overflow drain structure, for example.

[0002]

[Description of the Prior Art]Conventional technology is explained with reference to drawing 8 thru/or drawing 13. Drawing 8 is a sectional view of an important section, and drawing 9 is the impurity atom concentration profile figure of the depth direction of each impurity diffused layer which met the A'-A' cutout line in drawing 8, Drawing 10 is the impurity atom concentration profile figure of the depth direction of each impurity layer which met the B'-B' cutout line in drawing 8, Drawing 11 is a figure showing the potential profile of the depth direction of each impurity diffused layer which met the A'-A' cutout line and B'-B' cutout line in drawing 8, Drawing 12 is an impurity atom concentration profile figure corresponding to drawing 10 for explaining the conventional problem avoiding method, and drawing 13 is a figure showing the potential profile corresponding to drawing 11 for explaining the conventional problem avoiding method.

[0003]It is a solid state image pickup device which the photo-diode 2 of a photoelectric conversion part which generates an electric charge according to the light into which 1 entered in drawing 8 thru/or drawing 13 forms the isolation region 3 in between, for example, matrix form (the shape of two dimensions)

comes to arrange, Form the thin p type well 5 in the depths of the n-type semiconductor board 4, and in the upper part of the n-type semiconductor board 4 further The n type impurity diffusion zone 6, The p type impurity diffusion zone 7 is arranged to matrix form on the upper surface of this n type impurity diffusion zone 6, respectively, and the photo-diode 2 which forms a PN junction is formed in the boundary part of the n type impurity diffusion zone 6 and the p type impurity diffusion zone 7, and it is constituted.

[0004]And the p type impurity diffusion zone 7 is fixed to a GND level, the unstable surface 8 of combination is shielded by this, and generating of dark current is controlled. The reverse bias which makes the n-type semiconductor board 4 reverse the p type well 5 by being connected to a power supply is impressed, When generated by the excess charges which exceed the storage capacitance of the photo-diode 2 by superfluous incident light etc., these excess charges are swept out by the n-type semiconductor board 4, and serve as end-fire array overflow drain structure.

[0005]On the other hand, the 1st p type isolation impurity diffused layer 9 of predetermined impurity concentration is formed in a little deep depths which do not result by the p type well 5 from the surface 8 of the n-type semiconductor board 4 between the photo-diodes 2 with which the isolation region 3 adjoins.

[0006]On the photo-diode 2 and the n-type semiconductor board 4 with which

the isolation region 3 was formed, as the insulating layer 10 is passed in between, the transfer electrode wiring 11 and 12 is formed above the isolation region 3.

The light shielding layer 14 which carried out the opening of the window part 13 which incorporates incident light into photo-diode 2 portion is formed on the insulating layer 10.

[0007]The concentration distribution and the potential profile of an impurity in the depth direction of each impurity diffused layer in the photo-diode 2 and the isolation region 3, The portion in which it has become as shown in drawing 9, drawing 10, and drawing 11, and the photo-diode 2 was formed is what meets an A'-A' cutout line, The portion in which C_a' shows concentration distribution, and each curve of D_a' has shown the potential profile, and the isolation region 3 was formed meets a B'-B' cutout line, C_b' shows concentration distribution and each curve of D_b' has shown the potential profile.

[0008]And the impurity concentration of the portion in which the photo-diode 2 was formed, The peak part 7a of the left-hand side in drawing 9 in which concentration distribution C_a' is shown is the p type impurity diffusion zone 7 with the thing corresponding to [corresponding to the n type impurity diffusion zone 6 in the peak part 6a which adjoins this] the p type well 5 in the right-hand side

peak part 5a. On the other hand, the impurity concentration of the portion in which the isolation region 3 was formed is a thing corresponding to [corresponding to the 1st isolation impurity diffused layer 9 in the peak part 9b of the left-hand side in drawing 10 in which concentration distribution C_b' is shown] the p type well 5 in the right-hand side peak part 5a.

[0009]From the surface 8 to depth X_1', among potential profile D_a' in the formed parts of the photo-diode 2. Potential P_1' of the portion of the p type well 5 which hits an overflow drain is formed of the reverse bias voltage impressed to the n-type semiconductor board 4. The p type well 5 can be swept out to the n-type semiconductor board 4 as excess charges, when the electric charge exceeding this potential P_1' occurs in the photo-diode 2, since it had such potential P_1'.

[0010]The position of the depth direction of depth X_1' which is potential P_1' from this serves as a boundary in which an electric charge is stored. For this reason, since the depth direction position in which the p type well 5 is formed serves as a sensitization limit, in order to usually bring close to human being's spectral luminous efficacy, the p type well 5 is formed in the depths which serve as a depth of about 3 micrometers from the surface 8 of the n-type semiconductor board 4, for example so that the long wavelength sensitivity of the incident light may be obtained.

[0011]On the other hand, it is necessary to form the 1st isolation impurity

diffused layer 9 of the isolation region 3 in the depths of the n-type semiconductor board 4 for isolation. However, a field with the n-type semiconductor board 4 will produce between the p type wells 5 only in the 1st isolation impurity diffused layer 9.

[0012]For this reason, when the impurity concentration of the 1st formed isolation impurity diffused layer 9 is thin. From the surface 8 of potential profile D_b' which meets a B'-B' cutout line as shown in drawing 11 to depth X $_2$'. Potential P_2' deeper than depth X_1[of potential profile D_a' which meets the A'-A' cutout line of a position deeper than this] ', i.e., potential P_1' in p type well 5 portion, appears.

[0013]Since potential P_2' in depth X $_2$' is potential deeper than potential P_1' in depth X $_1$', when it is generated by excess charges with the photo-diode 2, It will mix in the photo-diode 2 which adjoins through the portion of deep potential P_2', and the electric charge which became superfluous will cause a blooming phenomenon, before being swept out by the n-type semiconductor board 4. In order to prevent such a problem, the reverse bias voltage impressed to the n-type semiconductor board 4 is raised, Potential P_1' in depth X $_1$[of potential profile D_a'] ' must be made deeper than potential P_2' in depth X $_2$[of potential profile D_b'] '. However, when it does in this way and the evasion in question is aimed at, the new problem that the amount of the maximum stored charge of the

photo-diode 2 will decrease will be produced.

[0014]In order to avoid the above problems, it is good to make deep impurity concentration of the 1st isolation impurity diffused layer 9. thereby -- an isolation region -- forming -- having had -- a portion -- an impurity -- concentration distribution -- drawing 10 -- B -- ' - B -- ' -- a cutout line -- meeting -- concentration distribution -- C -- $_b$ -- ' -- corresponding -- making -- being shown -- drawing 12 -- concentration distribution -- C -- $_b$ -- " -- like -- becoming. A potential profile becomes like potential profile D_b" of drawing 13 which is made to correspond to potential profile D_b' which meets the B'-B' cutout line of drawing 11, and is shown. Potential profile D_a' of the photo-diode formed parts in drawing 13 is the same as the thing of the formed parts of the photo-diode 2 which met the A'-A' cutout line of drawing 11. Peak part 9b' of the left-hand side in concentration distribution C_b" of drawing 12 corresponds to the 1st isolation impurity diffused layer of an isolation region.

[0015]By doing in this way, potential P_2" in depth X $_2$" from the substrate face of potential profile D_b", Rather than potential P_1[of depth X $_1$'] ' of potential profile D_a', will become shallow and potential deeper than potential P_1[of potential profile D_a'] ', It does not appear before depth X_1' from the same substrate face of potential profile D_b". For this reason, since it is not necessary to make high reverse bias voltage impressed to the n-type semiconductor board 4 for

controlling a blooming phenomenon, the problem that the amount of the maximum stored charge of the photo-diode 2 will decrease is avoidable.

[0016]However, in the above-mentioned conventional technology, if the impurity concentration of the 1st isolation impurity diffused layer 9 becomes deep, it will become difficult to change potential P_1' in depth X_1' from the surface 8 to the reverse bias voltage impressed to the n-type semiconductor board 4. In order to make deep potential P_1' of the p type well 5, it must stop thereby, having to impress high reverse bias voltage to the n-type semiconductor board 4. The electronic shutter mode which sweeps out temporarily altogether the electric charge accumulated in the inside of the photo-diode 2 to the n-type semiconductor board 4 will stop as a result, functioning.

[0017]Thus, since isolation of the adjoining photo-diode 2 by the isolation region 3 cannot fully carry out in a Prior art, When many electric charges occur, an electric charge mixes in the photo-diode 2 which adjoins before sweeping out excess charges to the n-type semiconductor board 4, and a blooming phenomenon occurs, or, Or if reverse bias voltage impressed to the n-type semiconductor board 4 is made high in order to control a blooming phenomenon, the amount of the maximum stored charge of the photo-diode 2 will decrease. In order to control a blooming phenomenon, when impurity concentration of the 1st isolation impurity diffused layer 9 is made deep, In order to sweep out all the

electric charges accumulated in the photo-diode 2 to the n-type semiconductor board 4, it must stop having to impress high reverse bias voltage, and an electronic shutter mode stops functioning.

[0018]

[Problem(s) to be Solved by the Invention]The positive separation by the isolation region of a photoelectric conversion part where the place which this invention was made in view of the above situations, and is made into the purpose adjoins, It is in providing the solid state image pickup device which enabled it to sweep out all the electric charges accumulated in the photoelectric conversion part to a semiconductor substrate without making reverse bias voltage high.

[0019]

[Means for Solving the Problem]A photoelectric conversion part which a solid state image pickup device of this invention is formed so that it may become predetermined arrangement in the upper part of a semiconductor substrate and a semiconductor substrate, and generates stored charge according to incident light, In a solid state image pickup device provided with an isolation region which separates this photoelectric conversion part, and the 1st impurity diffused layer that discharges excess charges by which it was generated in a photoelectric conversion part to that exterior, An isolation region is characterized by having

the 3rd impurity diffused layer under the 2nd impurity diffused layer and the 2nd impurity diffused layer, and a photoelectric conversion part is further arranged in the shape of two dimensions, and. It is a thing, wherein the 3rd impurity diffused layer is provided so that a directly under field of a photoelectric conversion part may be surrounded, The 3rd impurity diffused layer is the thing currently forming in a prescribed depth part from the surface in a semiconductor substrate in the shape of an approximately lattice, A position which shows maximum peak concentration in an impurity profile of the 2nd impurity diffused layer, It is a thing being a position and an approximately same depth position which show the maximum potential of a photoelectric conversion part, The 3rd impurity diffused layer is characterized by being provided in a position of depth direction distance of approximately middle of the 2nd impurity diffused layer and the 1st impurity diffused layer, and further it the 3rd impurity diffused layer, It is the same pattern as the 2nd impurity diffused layer.

[0020]

[Embodiment of the Invention]one embodiment of following this invention -- drawing 1 -- or the drawing 7 reference is carried out and it explains. Drawing 1 is a sectional view of an important section, and drawing 2 is the impurity atom concentration profile figure of the depth direction of each impurity diffused layer which met the A-A cutout line in drawing 1, Drawing 3 is the impurity atom

concentration profile figure of the depth direction of each impurity diffused layer which met the B-B cutout line in drawing 1, Drawing 4 is a figure showing the potential profile of the depth direction of each impurity diffused layer which met the A-A cutout line and B-B cutout line in drawing 1, It is a sectional view shown in order that drawing 5 may explain the morphosis of the 1st isolation impurity diffused layer and the 2nd isolation impurity diffused layer, Drawing 6 is a top view showing the pattern of the 1st isolation impurity diffused layer and the 2nd isolation impurity diffused layer, and drawing 7 is a top view showing the pattern of the 1st isolation impurity diffused layer in a modification gestalt, and the 2nd isolation impurity diffused layer.

[0021]It is a solid state image pickup device which the photo-diode 22 of a photoelectric conversion part which generates an electric charge according to the light into which 21 entered in drawing 1 thru/or drawing 7 forms the isolation region 23 in between, for example, matrix form (the shape of two dimensions) comes to arrange, So that sensitivity may be obtained to the long wavelength of the incident light in order to bring close to human being's spectral luminous efficacy, the depths, for example, the sensitization limit, of the n-type semiconductor board 24, Form the thin p type well 27 in a depth of about 3 micrometers from the substrate face 26, and in the upper part of the n-type semiconductor board 24 further The n type impurity diffusion zone 28, The p

type impurity diffusion zone 29 is arranged to matrix form on the upper surface of this n type impurity diffusion zone 28, respectively, and the photo-diode 22 which forms a PN junction is formed in the boundary part of the n type impurity diffusion zone 28 and the p type impurity diffusion zone 29, and it is constituted.

[0022]The 1st p type isolation impurity diffused layer 30 is formed in the upper part of the n-type semiconductor board 24 between the photo-diodes 22 contiguous to the isolation region 23. . And the maximum density position of this 1st p type isolation impurity diffused layer 30 does not result by the p type well 27 from the substrate face 26. depth X_4 of the position of maximum potential P_4 of the photo-diode 22 -- abbreviated -- it is in prescribed depth X_{3b} which becomes the same -- the direction in every direction -- respectively -- a predetermined pitch -- alienation -- it is arranged, and it is formed so that the prescribed pattern shown in drawing 6 may be made.

[0023]Furthermore in the isolation region 23, the omitted portion between the p type well 27 in the n-type semiconductor board 24, and the 1st isolation impurity diffused layer 30, For example, the 2nd p type isolation impurity diffused layer 31 that has maximum density in depth X_{2b} of the position of abbreviated 1 / 2 is formed so that the same pattern as the 1st p type isolation impurity diffused layer 30 may be made.

[0024]The position of the depth direction in the n-type semiconductor board 24

which forms the 2nd p type isolation impurity diffused layer 31 should just be between the p type well 27 and the 1st p type isolation impurity diffused layer 30 with the dose of the impurity of the 2nd p type isolation impurity diffused layer 31, etc.

[0025]And the p type impurity layer 29 is fixed to a GND level, the unstable substrate face 26 of combination is shielded by this, and generating of dark current is controlled. The reverse bias which makes the n-type semiconductor board 24 reverse the p type well 27 by being connected to a power supply is impressed, When generated by the excess charges which exceed the storage capacitance of the photo-diode 22 by superfluous incident light etc., these excess charges have formed the end-fire array overflow drain structure swept out by the n-type semiconductor board 24.

[0026]On the photo-diode 22 and the n-type semiconductor board 24 with which the isolation region 23 was formed, The light shielding layer 36 which carried out the opening of the window part 35 which the transfer electrode wiring 33 and 34 is formed above the isolation region 23 as the insulating layer 32 is passed in between, and also incorporates incident light into photo-diode 22 portion on the insulating layer 32 is formed.

[0027]The concentration distribution and the potential profile of an impurity, [in / at what was constituted in this way / the depth direction of each impurity diffused

layer in the photo-diode 22 and the isolation region 23] The portion in which it has become as shown in drawing 2, drawing 3, and drawing 4, and the photo-diode 22 was formed is what meets an A-A cutout line, The portion in which C_a shows concentration distribution, and each curve of D_a has shown the potential profile, and the isolation region 23 was formed meets a B-B cutout line, C_b shows concentration distribution and each curve of D_b has shown the potential profile.

[0028]And the impurity concentration of the portion in which the photo-diode 22 was formed, The peak part 29a of the left-hand side in drawing 2 in which concentration distribution C_a is shown is the p type impurity diffusion zone 29 with the thing corresponding to [corresponding to the n type impurity diffusion zone 28 in the peak part 28a which adjoins this] the p type well 27 in the right-hand side peak part 27a. On the other hand, the impurity concentration of the portion in which the isolation region 23 was formed, The peak part 30b of the left-hand side in drawing 3 in which concentration distribution C_b is shown is a thing corresponding to [corresponding to the 2nd p type isolation impurity diffused layer 31 in the peak part 31b which adjoins this at the 1st p type isolation impurity diffused layer 30] the p type well 27 in the right-hand side peak part 27a.

[0029]From the substrate face 26 to depth X_1, among potential profile D_a in the

formed parts of the photo-diode 22. Potential P_1 of the portion of the p type well 27 which hits an overflow drain is formed of the reverse bias voltage impressed to the n-type semiconductor board 24. On the other hand, since the 2nd p type isolation impurity diffused layer 31 of prescribed concentration is formed between the 1st p type isolation impurity diffused layer 30 and the p type well 27, in the isolation region 23, From the substrate face 26 to depth X_2 and X_3 of potential profile D_b which meet the B-B cutout line shown in drawing 4. Potential P_2 shallower than potential P_1 and P_3 of depth X_1 of potential profile D_a which meets the A-A cutout line of a position deeper than this appear. As a result, when the electric charge which exceeds potential P_1 to the photo-diode 22 occurs, the electric charge which became superfluous will be swept out by the n-type semiconductor board 24 exceeding potential P_1.

[0030]And, without lessening the amount of the maximum stored charge of the photo-diode 22, since it has the above composition, Before excess charges are swept out by the n-type semiconductor board 24, the blooming phenomenon which an electric charge mixes in the photo-diode 22 which adjoins from a position shallower than depth X_1, and is generated can be controlled. Since it is not necessary to increase the impurity concentration of the 1st p type isolation impurity diffused layer 30, it becomes unnecessary to consider it as what also has the high reverse bias voltage impressed to the n-type semiconductor board

24 in order to make deep potential P_1 of the p type well 27. And the electronic shutter mode which sweeps out temporarily altogether the electric charge accumulated in the inside of the photo-diode 22 to the n-type semiconductor board 24 can also be made to function normally.

[0031]In order to form the 1st p type isolation impurity diffused layer 30 and the 2nd p type isolation impurity diffused layer 31 as mentioned above in the n-type semiconductor board 24 of the p type well 27 upper part in the isolation region 23, well-known photo etching art and high acceleration ion implantation art are used. That is, after forming the oxide film 37 for buffers in the n-type semiconductor board 24 upper surface in which the p type well 27 was formed, the upper surface is made to deposit the photoresist film 38. Next, the predetermined resist film pattern 40 which etches the deposited photoresist film 38 by patterning using a photo-etching method, devotes itself to the formation position of the p type 1st and the 2nd isolation impurity diffused layer 30 and 31 as shown in drawing 5, and has the opening 39 is formed.

[0032]Then, placing of boron (B) ion in high accelerating voltage is performed to the formation position of the 2nd p type isolation impurity diffused layer 31 of the n-type semiconductor board 24 to a prescribed depth via the placing opening 39 of the resist film pattern 40. By the separated process which changed ion implantation conditions, a boron ion is driven into the formation position of the

1st p type isolation impurity diffused layer 30 to a prescribed depth with the same resist film pattern 40.

[0033]Then, after removing the resist film pattern 40, heat treatment which served as annealing is performed, an impurity is diffused, and the 1st p type isolation impurity diffused layer 30 and the 2nd p type isolation impurity diffused layer 31 are formed in the n-type semiconductor board 24. The solid state image pickup device 21 shown in drawing 1 is formed through a well-known manufacturing process after that. About a formation order of the 1st p type isolation impurity diffused layer 30 and the 2nd p type isolation impurity diffused layer 31, the above may be reverse.

[0034]By manufacturing through the above high acceleration ion implantation processes, formation of the 1st p type isolation impurity diffused layer 30 and the 2nd p type isolation impurity diffused layer 31, It can carry out to the appropriate position made necessary [in the n-type semiconductor board 24], and the solid state image pickup device 21 which has the above-mentioned effect can be obtained.

[0035]In the above-mentioned embodiment, although the pattern of the 1st p type isolation impurity diffused layer 30 and the 2nd p type isolation impurity diffused layer 31 is made into the same thing, It may be made to provide 2nd p type isolation impurity diffused layer 31' for the pattern formed in the shape of

[containing the pattern of this 1st p type isolation impurity diffused layer 30] a lattice to the 1st p type isolation impurity diffused layer 30 like the modification gestalt shown in drawing 7. By thus, the thing for which it shall have a pattern of the shape of a lattice which surrounds the directly under field of the photo-diode 22 for 2nd p type isolation impurity diffused layer 31'. Blooming which the electric charge from the adjacent photo-diode 22 which sandwiched the vertical transfer path lower part other than the above-mentioned effect mixes and produces can be prevented.

[0036]Although arrangement of the photo-diode 22 was made into the shape of two dimensions (matrix form) in the above-mentioned embodiment, the effect same also as the shape of one dimension can be acquired again.

[0037]

[Effect of the Invention]According to this invention, the effect of being able to sweep out all the electric charges which could perform positive separation of the photoelectric conversion part which adjoins by an isolation region, and were accumulated in the photoelectric conversion part to a semiconductor substrate, without making reverse bias voltage high is done so so that clearly from the above explanation.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a sectional view of an important section showing one embodiment of this invention.

[Drawing 2]It is the impurity atom concentration profile figure of the depth direction of each impurity diffused layer which met the A-A cutout line in drawing 1.

[Drawing 3]It is the impurity atom concentration profile figure of the depth

direction of each impurity diffused layer which met the B-B cutout line in drawing 1.

[Drawing 4]It is a figure showing the potential profile of the depth direction of each impurity diffused layer which met the A-A cutout line and B-B cutout line in drawing 1.

[Drawing 5]It is a sectional view shown in order to explain the morphosis of the 1st isolation impurity diffused layer in one embodiment of this invention, and the 2nd isolation impurity diffused layer.

[Drawing 6]It is a top view showing the pattern of the 1st isolation impurity diffused layer in one embodiment of this invention, and the 2nd isolation impurity diffused layer.

[Drawing 7]It is a top view showing the pattern of the 1st isolation impurity diffused layer in the modification gestalt of one embodiment of this invention, and the 2nd isolation impurity diffused layer.

[Drawing 8]It is a sectional view of an important section showing conventional technology.

[Drawing 9]It is the impurity atom concentration profile figure of the depth direction of each impurity diffused layer which met the A'-A' cutout line in drawing 8.

[Drawing 10]It is the impurity atom concentration profile figure of the depth

direction of each impurity diffused layer which met the B'-B' cutout line in drawing 8.

[Drawing 11]It is a figure showing the potential profile of the depth direction of each impurity diffused layer which met the A'-A' cutout line and B'-B' cutout line in drawing 8.

[Drawing 12]It is an impurity atom concentration profile figure corresponding to drawing 10 for explaining the conventional problem avoiding method.

[Drawing 13]It is a figure showing the potential profile corresponding to drawing 11 for explaining the conventional problem avoiding method.

[Description of Notations]

22 -- Photo-diode

23 -- Isolation region

24 -- N-type semiconductor board

27 -- P type well

28 -- N type impurity diffusion zone

30 -- 1st p type isolation impurity diffused layer

31 31' -- 2nd p type isolation impurity diffused layer